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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,451	12/20/2005	Jose De Jesus Pineda De Gyvez	NL 030713	6439

65913 7590 12/31/2007

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EXAMINER
CHARIOUI, MOHAMED

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
12/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,451	PINEDA DE GYVEZ ET AL.	
	Examiner	Art Unit	
	Mohamed Charioui	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C § 133) Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Reynick (U.S. Patent No. 6,714,032).

As per claims 1-3 and 11, Reynick teaches applying a plurality of different DC power supply voltages to a circuit component under test, at least one of said power supply voltages being arranged to cause at least some of the elements of the circuit or component under test to operate in a predetermined region of operation; and measuring the quiescent current of said circuit or component as a result of application of said power supply voltages to generate a current signature representative of the operation of said circuit or component (see col. 6, lines 10-56 and col. 11, lines 14-40), the method being characterized in that said power supply voltages at which said quiescent current measurements are taken comprise selected distinct voltages, and comparing said generated current signature with a predetermined current signature representative of operation of a fault-free component or circuit so as to determine whether or not any faults are present in the component or circuit under test (see col. 6, lines 57-67).

As per claims 4 and 5, Reynick further teaches providing a single supply voltage means and ramping said supply voltage up to attain each of said selected power supply voltages, prior to measurement of the quiescent current (see col. 13, lines 25-58).

As per claim 6, Reynick further teaches a fault dictionary database is provided, and the method includes the further step of comparing a generated current signature with contents of such a database to diagnose one or more faults present in the circuitry under test (see col. 7, lines 20-46 and col. 8, lines 14-24).

As per claims 7 and 8, Reynick further teaches a tolerance window is defined for the resultant quiescent current measurements for at least one the selected power supply voltages (see col. 8, lines 25-39 and col. 10, lines 10-40).

As per claims 9 and 10, Reynick further teaches a computer program for enabling the method of claim 1 to be performed (see col. 16, lines 32-46 and col. 20, lines 17-23).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reynick in view of Nakano et al. (U.S. Patent No. 7,109,558).

Reynick teaches the system as stated above except that the different DC power supply voltages are selected to cause at least some of the elements of the circuit or component under test to pass through subthreshold, linear and saturation operating regions.

Nakano et al. teach this feature (see col. 18, lines 35-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Nakano et al.'s teaching into Reynick's teaching because it monitor the circuit elements as they pass through linear an saturation regions. Therefore, determination of whether the circuit elements are defective or not would be made.

Response to Arguments

3. Applicant's arguments filed 9/28/07 have been fully considered but they are not persuasive.

Applicant argues that Reynick does not disclose applying multiple different electrical stimuli on the integrated circuit.

Examiner disagrees with Applicant's argument because Reynick teaches that a plurality of vectors (i.e. voltages) are applied to the DUT (see col. 4, lines 54-67; col. 10, lines 2-10; and col. 9, lines 50-60).

Applicant argues that Reynick does not disclose the step of providing a single supply voltage means and ramping said voltage up to attain each of said selected power supply voltages, prior to measurement of the quiescent current.

Examiner disagrees with Applicant's argument because Reynick teaches this feature (see col. 13, lines 28-58 and Fig. 3). The Examiner considers ramping up the supply power to be increasing the power supply.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Charioui whose telephone number is (571) 272-2213. The examiner can normally be reached Monday through Friday, from 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohamed Charioui

12/21/07

Edward Raymond

EDWARD RAYMOND
PRIMARY EXAMINER